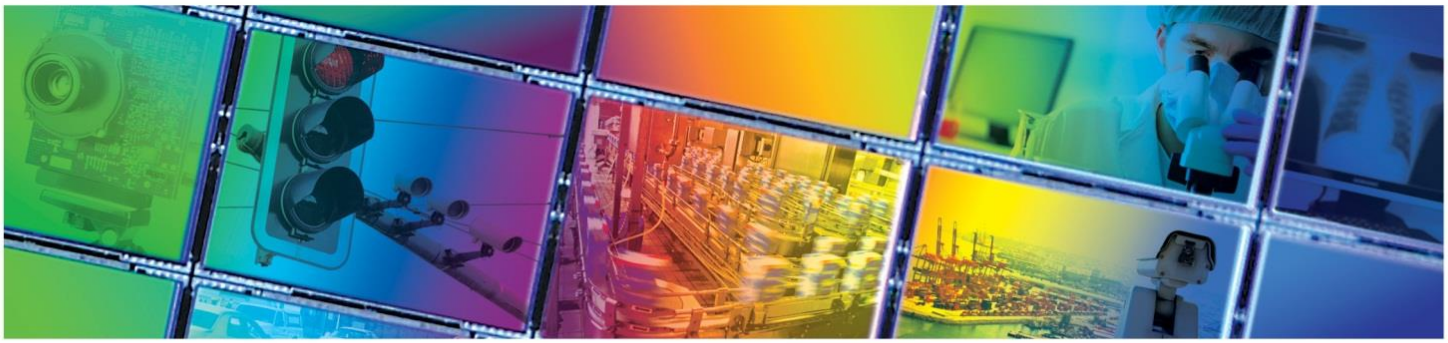
ON Semiconductor®

KAI-1010 IMAGE SENSOR

1008 (H) X 1018 (V) INTERLINE CCD IMAGE SENSOR



JUNE 9, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0021

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

Summary Specification

KAI-1010 Image Sensor

DESCRIPTION

The KAI-1010 Image Sensor is a high-resolution monochrome charge coupled device (CCD) device whose non-interlaced architecture makes it ideally suited for video, electronic still and motion/still camera applications. The device is built using an advanced true two-phase, double-polysilicon, NMOS CCD technology. The p+npn- photodetector elements eliminate image lag and reduce image smear while providing antiblooming protection and electronic-exposure control. The total chip size is 10.15 (H) mm x 10.00 (V) mm.

FEATURES

- Front Illuminated Interline Architecture
- Progressive Scan (Non-interlaced)
- Electronic Shutter
- On-Chip Dark Reference Pixels
- Low Dark Current
- High Sensitivity Output Structure
- Dual Output Shift Registers
- Antiblooming Protection
- Negligible Lag
- Low Smear (0.01% with microlens)

APPLICATIONS

- Machine Vision

Parameter	Typical Value
Architecture	Interline CCD, Non-Interlaced
Total Number of Pixels	1024 (H) x 1024 (V)
Number of Effective Pixels	1008 (H) x 1018 (V)
Number of Active Pixels	1008 (H) x 1018 (V)
Number of Outputs	1 or 2
Pixel Size	9 µm (H) x 9 µm (V)
Active Image Size	9.1 mm (H) x 9.2 mm (V) 12.9 mm (diagonal)
Optical Fill-Factor	60%
Saturation Signal	>50,000 electrons
Output Sensitivity	12 µV/electron
Dark Noise	50 electrons rms
Dark Current	<0.5 nA/cm^2
Quantum Efficiency (wavelength = 500 nm)	37%
Blooming Suppression	>100 X
Maximum Data Rate	20 MHz/Channel (2 channels)
Image Lag	Negligible
Package	CERDIP
Cover Glass	AR Coated (both sides)

All parameters above are specified at T = 40 °C

Ordering Information

Catalog Number	Product Name	Description	Marking Code
2H4115	KAI- 1010-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	KAI-1010M Serial Number
2H4614	KAI- 1010-ABA-CD-BA	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	KAI-1010M Serial Number
2H4121	KAI- 1010-ABA-CR-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	KAI-1010M Serial Number
2H4613	KAI- 1010-ABA-CR-BA	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Standard Grade	KAI-1010M Serial Number

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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1964 Lake Avenue
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Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

Device Description

Architecture

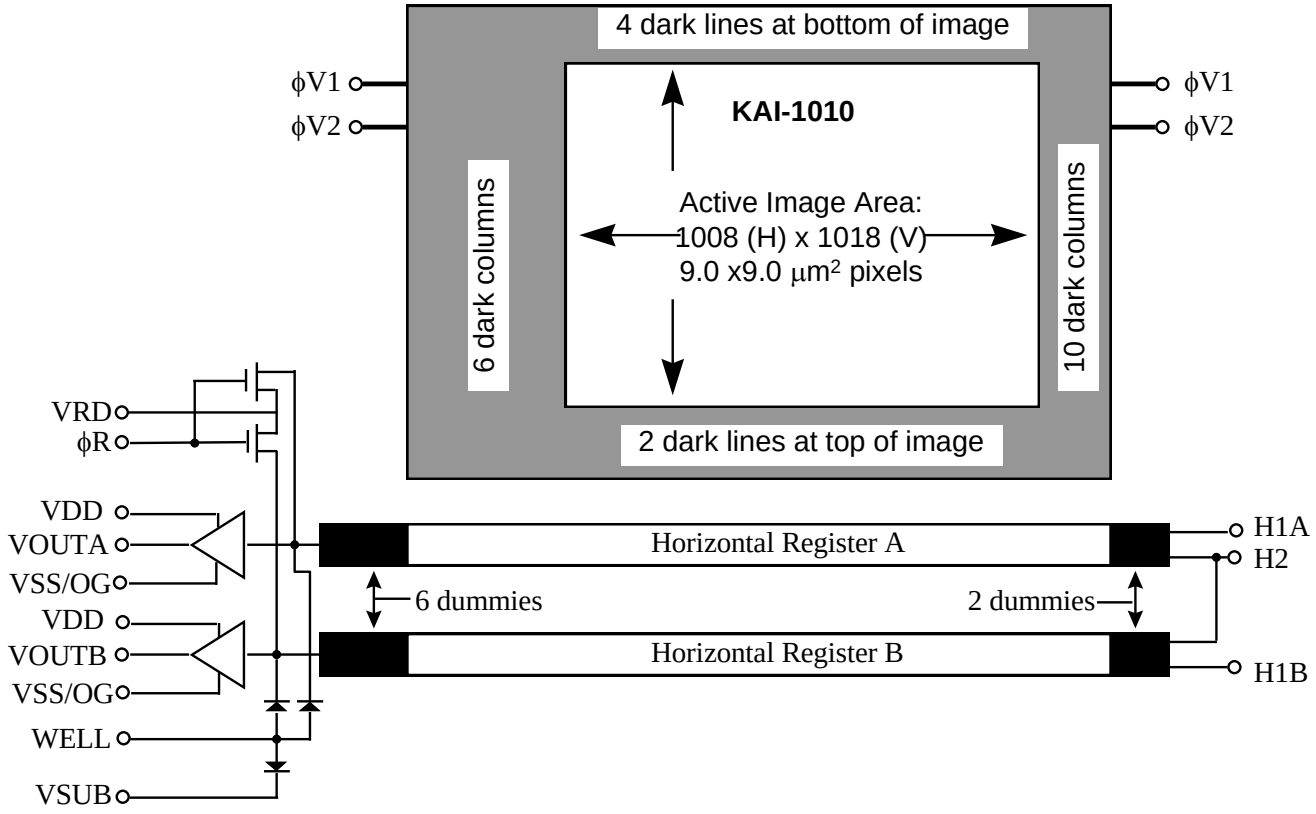


Figure 1: Functional Block Diagram

The KAI-1010 consists of 1024 x 1024 photodiodes, 1024 vertical (parallel) CCD shift registers (VCCDs), and dual 1032 pixel horizontal (serial) CCD shift registers (HCCDs) with independent output structures. The device can be operated in either single or dual line mode. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The active pixels are arranged in a 1008 (H) x 1018 (V) array with an additional 16 columns and 6 rows of light-shielded dark reference pixels.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

CHARGE TRANSPORT

The accumulated or integrated charge from each photodiode is transported to the output by a three step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock (φV1). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock, φH2, these charge packets are dumped over the output gate (OG, Figure 3) onto the floating diffusion (FDA and FDB, Figure 3).

Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the HCCDs begins when φV2 is clocked high and then low (while holding øH1A high) causing charge to be transferred from φV1 to φV2 and subsequently into the A HCCD. The A register can now be read out in single line mode. If it is desired to operate the device in a dual line readout mode for higher frame rates, this line is transferred into the B HCCD by clocking φH1A to a low state, and φH1B to a high state while holding φH2 low. After φH1A is returned to a high state, the next line can be transferred into the A HCCD. After this clocking sequence, both HCCDs are read out in parallel.

The charge capacity of the horizontal CCDs is slightly more than twice that of the vertical CCDs. This feature allows the user to perform two-to-one line aggregation in the charge domain during V-to-H transfer. This device is also equipped with a fast dump feature that allows the user to selectively dump complete lines (or rows) of pixels at a time. This dump, or line clear, is also accomplished during the V-to-H transfer time by clocking the fast dump gate.

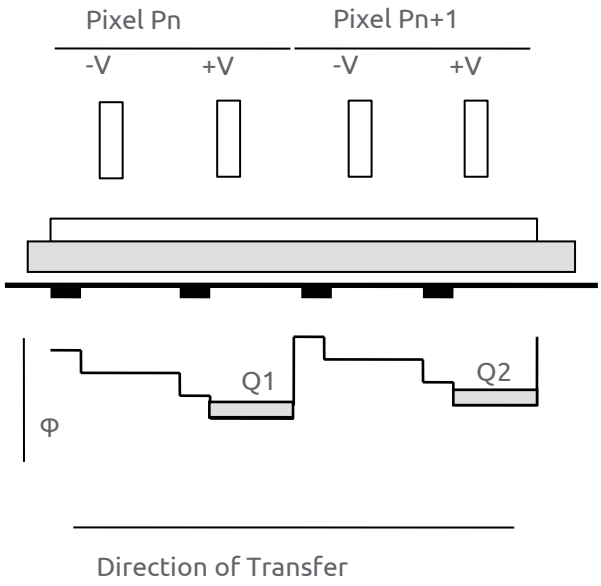


Figure 2: True 2 Phase CCD Cross Section

OUTPUT STRUCTURE

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression ΔVfd=ΔQ/Cfd. A three stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of μV/e^-. After the signal has been sampled off-chip, the reset clock (φR) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage (VRD).

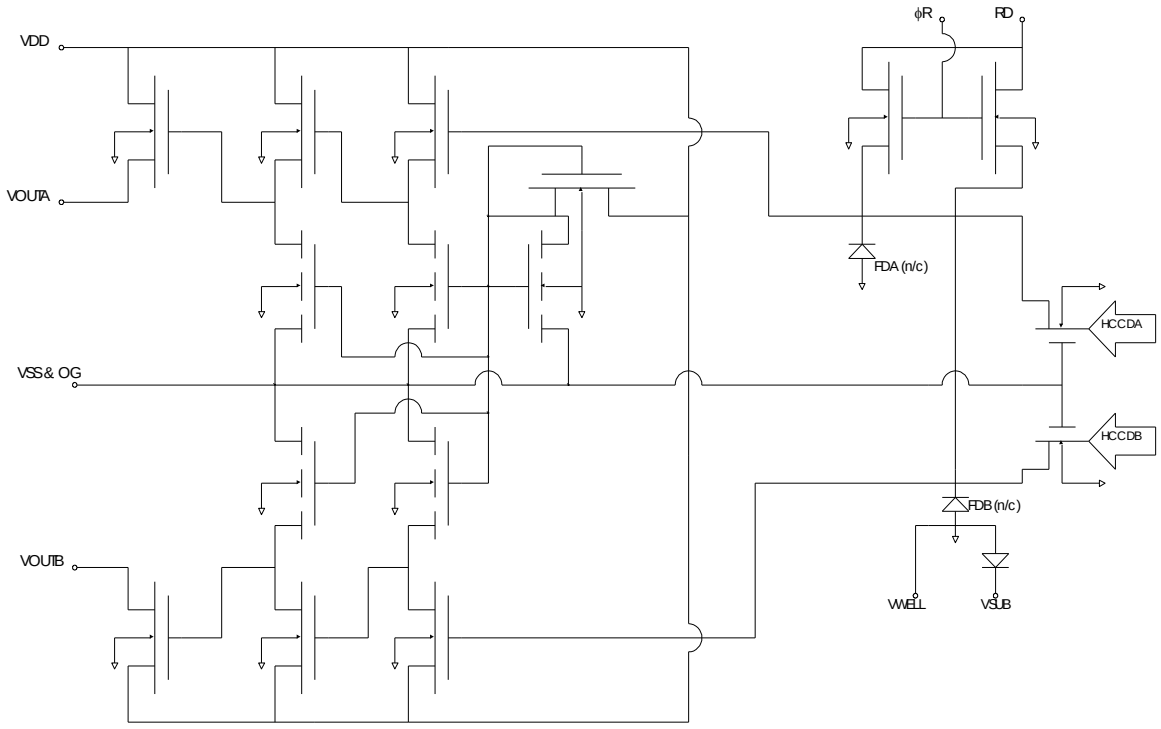


Figure 3: Output Structure

ELECTRONIC SHUTTER

The KAI-1010 provides a structure for the prevention of blooming which may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD). This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse (VES ≈ 40V) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on φV1. The integration time is then the time between the falling edges of the substrate shutter pulse and φV1. This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feed-through. The shutter pulse VES must be “hidden” in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

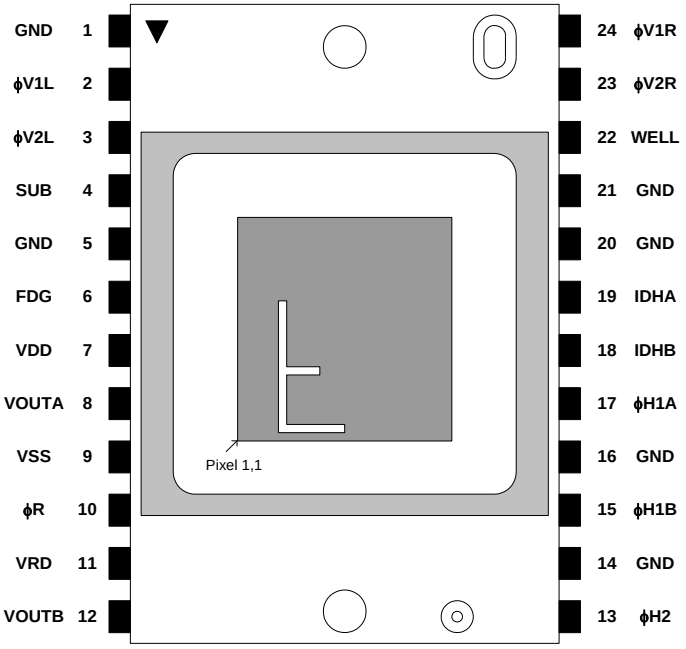


Figure 4: Pinout Diagram

PIN	NAME	DESCRIPTION	Notes
1,5,14,16,20,21	GND	Ground	1
2, 24	φV1	Vertical CCD Clock - Phase 1	2
3, 23	φV2	Vertical CCD Clock - Phase 2	3
4	SUB	Substrate	
6	FDG	Fast Dump Gate	
7	VDD	Output Amplifier Supply	
8	VOUTA	Video Output Channel A	
9	VSS	Output Amplifier Return & OG	
10	φR	Reset Clock	
11	VRD	Reset Drain	
12	VOUTB	Video Output Channel B	
13	φH2	A & B Horizontal CCD Clock - Phase 2	
15	φH1B	B Horizontal CCD Clock - Phase 1	
17	φH1A	A Horizontal CCD Clock - Phase 1	
18	IDHB	Input Diode B Horizontal CCD	
19	IDHA	Input Diode A Horizontal CCD	
22	WELL	P-Well	

Notes:
1. All GND pins should be connected to WELL (P-Well).
2. Pins 2 and 24 must be connected together - only 1 Phase 1 clock driver is required.
3. Pins 3 and 23 must be connected together - only 1 Phase 2 clock driver is required.

Imaging Performance

All the following values were derived using nominal operating conditions using the recommended timing. Unless otherwise stated, readout time = 140 ms, integration time = 140 ms and sensor temperature = 40 °C. Correlated double sampling of the output is assumed and recommended. Many units are expressed in electrons, to convert to voltage, multiply by the amplifier sensitivity.

Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

ELECTRO-OPTICAL FOR KAI-1010-ABA

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
F F	Optical Fill Factor		55.0		%	
Esat	Saturation Exposure		0.037		$\mu J/cm^2$	1
QE	Peak Quantum Efficiency		37		%	2
PRNU	Photoresponse Non-uniformity		10.0		%pp	3, 4
PRNL	Photoresponse Non-linearity		5.0		%	

Table 1: Electro-Optical Image Specifications KAI-1010-ABA

Notes:

1. For λ = 550nm wavelength, and Vsat = 350 mV.
2. Refer to typical values from Figure 5.
3. Under uniform illumination with output signal equal to 280 mV.
4. Units: % Peak to Peak. A 200 by 200 sub ROI is used.

MONOCHROME WITH MICROLENS QUANTUM EFFICIENCY

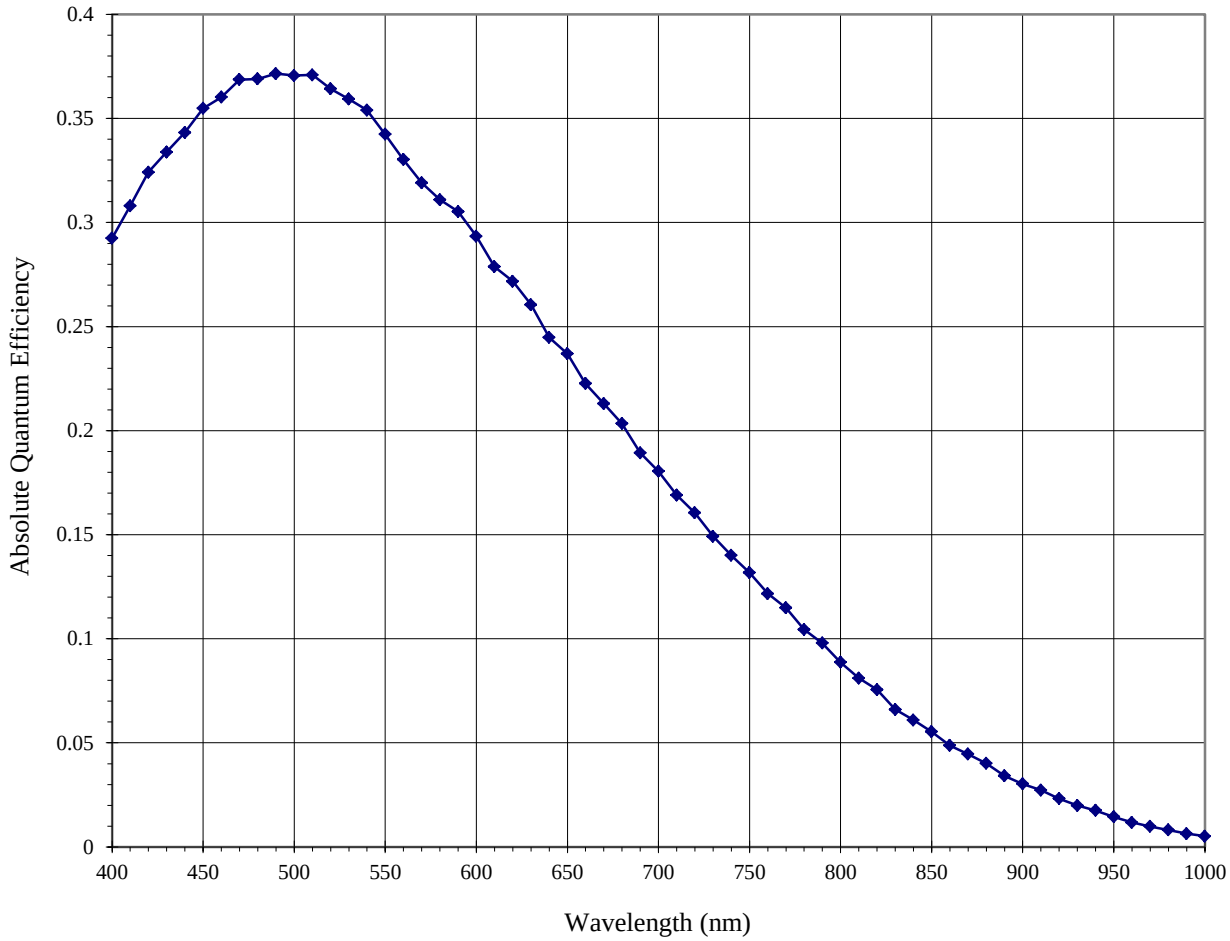


Figure 5: Nominal KAI-1010-ABA Spectral Response

ANGULAR QUANTUM EFFICIENCY

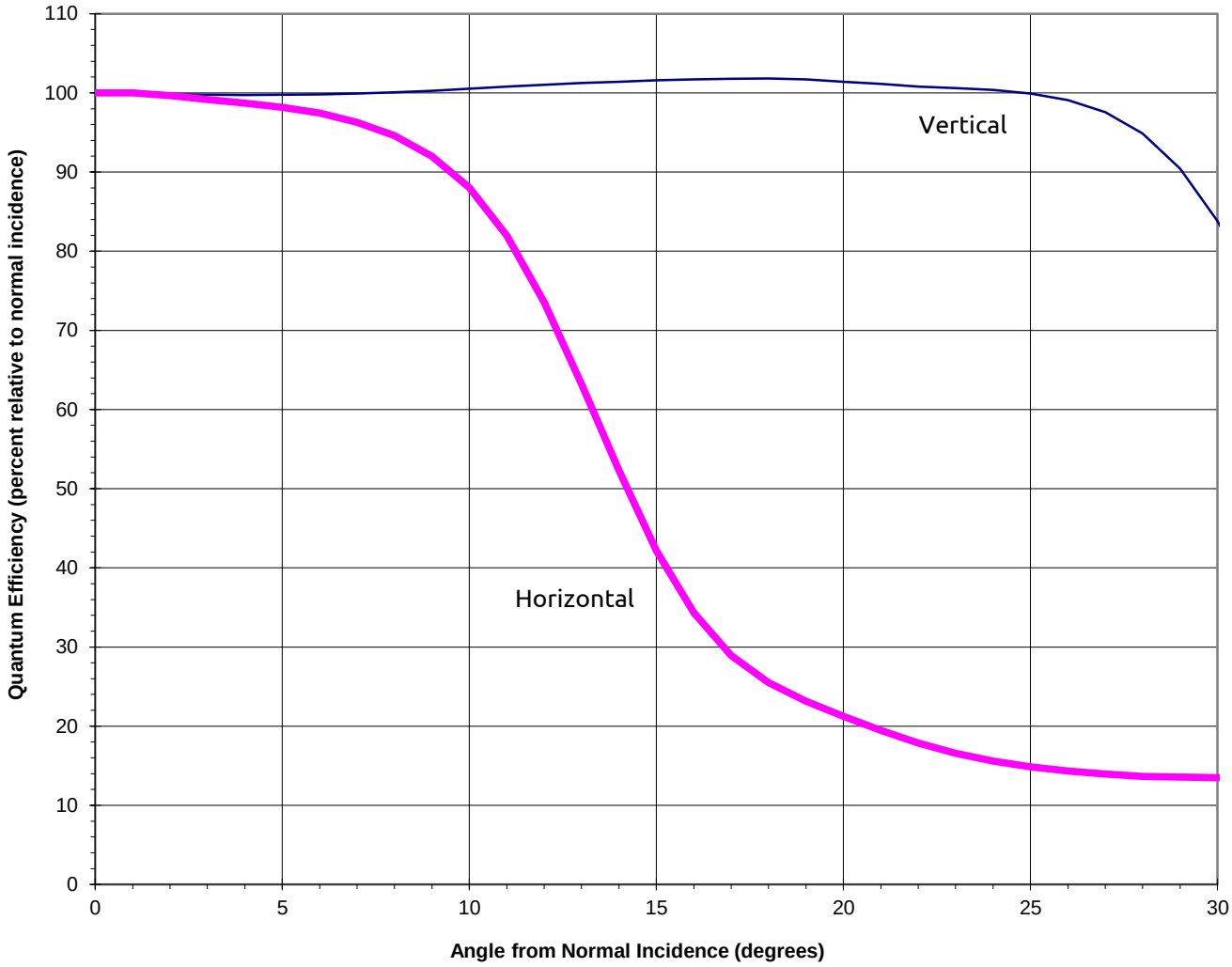


Figure 6: Angular Dependence of Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

FRAME RATES

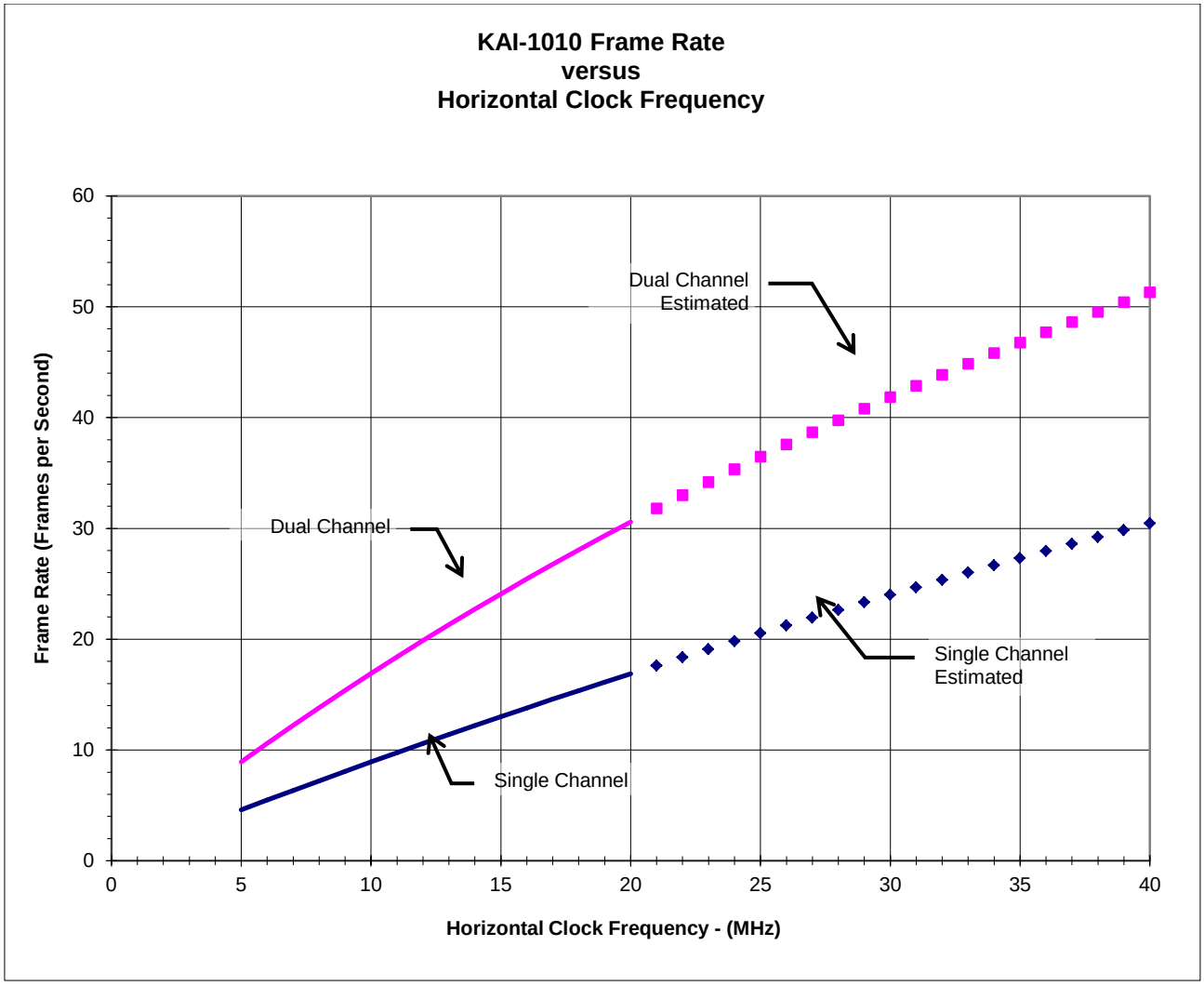


Figure 7: Frame Rate versus Horizontal Clock Frequency

CCD Image Specifications

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vsat	Output Saturation Voltage		350		mV	1,2,8
I_d	Dark Current			0.5	nA	
DCDT	Dark Current Doubling Temp	7	8	10	°C	
CTE	Charge Transfer Efficiency		0.99999			2,3
f_H	Horizontal CCD Frequency			40	MHz	4
IL	Image Lag			100	e^-	5
Xab	Blooming Margin			100		6,8
Smr	Vertical Smear		0.01		%	7

Table 2: CCD Image Specifications

Notes:

1. Vsat is the green pixel mean value at saturation as measured at the output of the device with Xab=1. Vsat can be varied by adjusting Vsub.
2. Measured at sensor output.
3. With stray output load capacitance of C_L = 10 pF between the output and AC ground.
4. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
5. This is the first field decay lag measured by strobe illuminating the device at (Hsat, Vsat), and by then measuring the subsequent frame's average pixel output in the dark.
6. Xab represents the increase above the saturation-irradiance level (Hsat) that the device can be exposed to before blooming of the vertical shift register will occur. It should also be noted that Vout rises above Vsat for irradiance levels above Hsat, as shown in Figure 8.
7. Measured under 10% (~ 100 lines) image height illumination with white light source and without electronic shutter operation and below Vsat.
8. It should be noted that there is tradeoff between Xab and Vsat.

Output Amplifier @ VDD = 15 V, VSS = 0.0 V

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vodc	Output DC Offset		7		V	1,2
P_d	Power Dissipation	----	225	----	mW	3
f_{-3db}	Output Amplifier Bandwidth		140		MHz	1,4
CL	Off-Chip Load			10	pF	

Table 3: Output Amplifier Image Specifications

Notes:

1. Measured at sensor output with constant current load of I_{out} = 5 mA per output.
2. Measured with VRD = 9 V during the floating-diffusion reset interval, (φR high), at the sensor output terminals.
3. Both channels.
4. With stray output load capacitance of C_L = 10 pF between the output and AC ground.

General

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNITS	NOTES
Vn - total	Total Sensor Noise		0.5		mV, rms	1
DR	Dynamic Range			60	dB	2

Table 4: General Image Specifications

Notes:
1. Includes amplifier noise and dark current shot noise at data rates of 10 MHz. The number is based on the full bandwidth of the amplifier. It can be reduced when a low pass filter is used.
2. Uses 20LOG(Vsat/Vn - total) where Vsat refers to the output saturation signal.

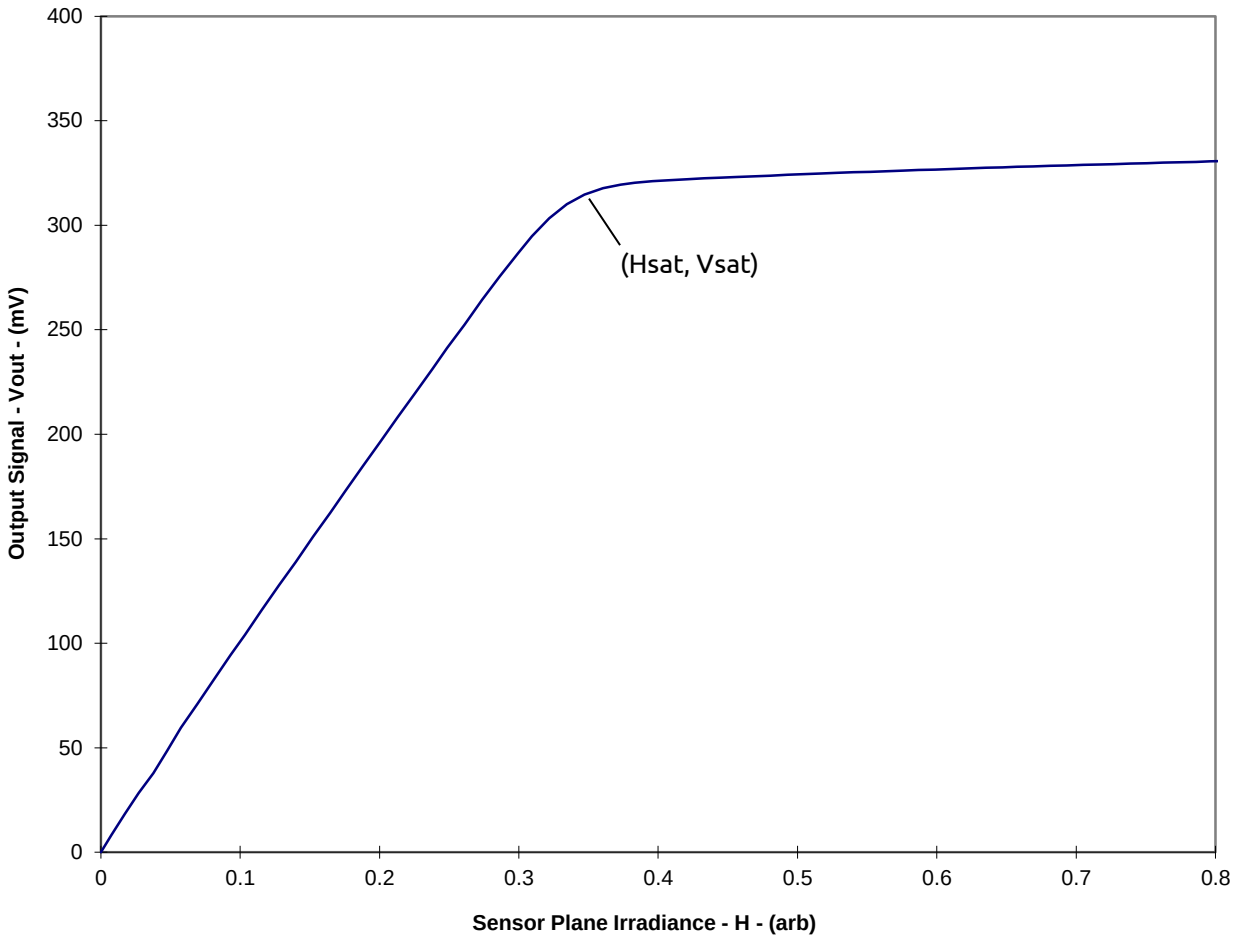


Figure 8: Typical KAI-1010-ABA Photoresponse

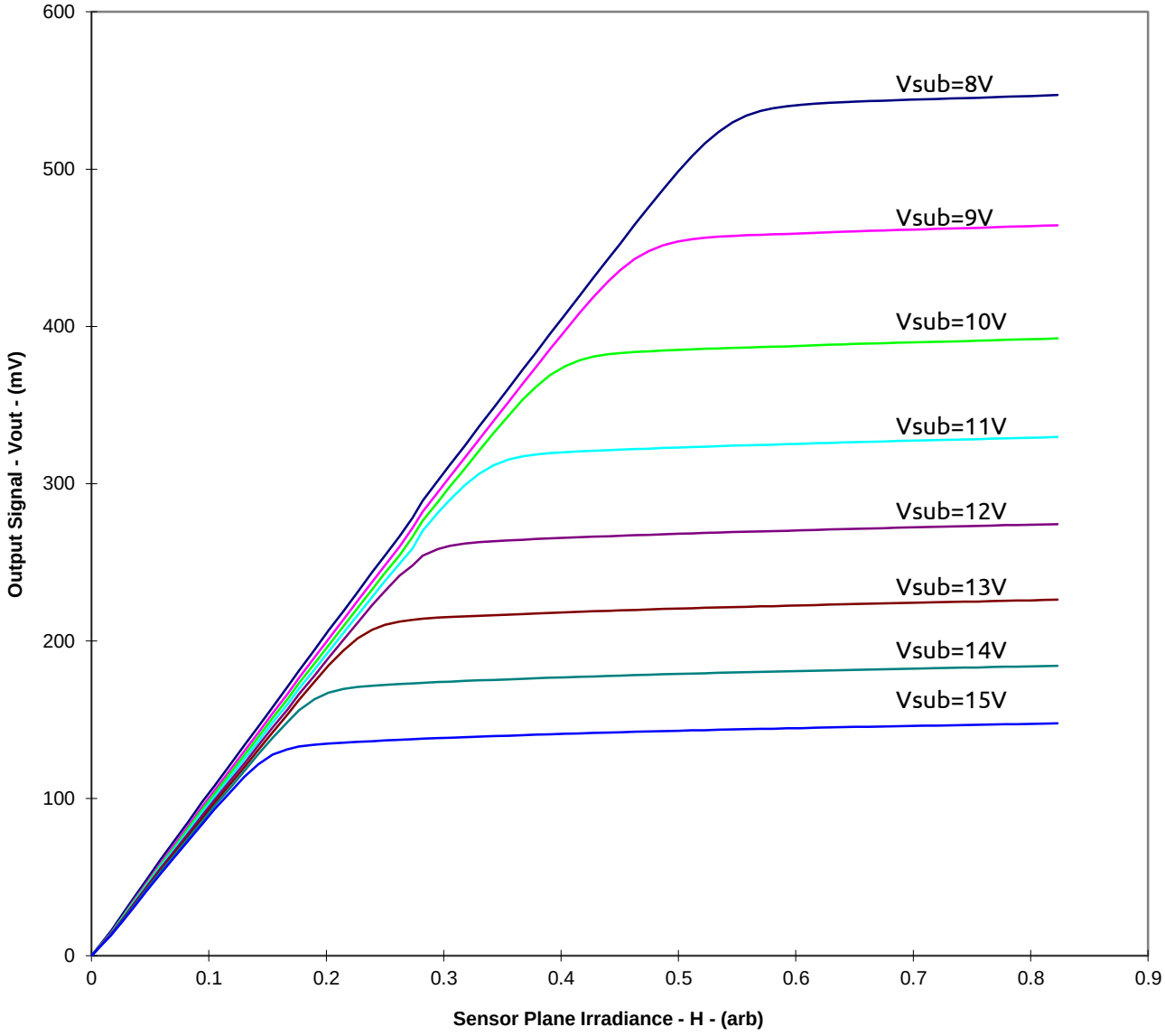


Figure 9: Example of Vsat versus Vsub

As Vsub is decreased, Vsat increases and anti-blooming protection decreases.

As Vsub is increased, Vsat decreases and anti-blooming protection increases.

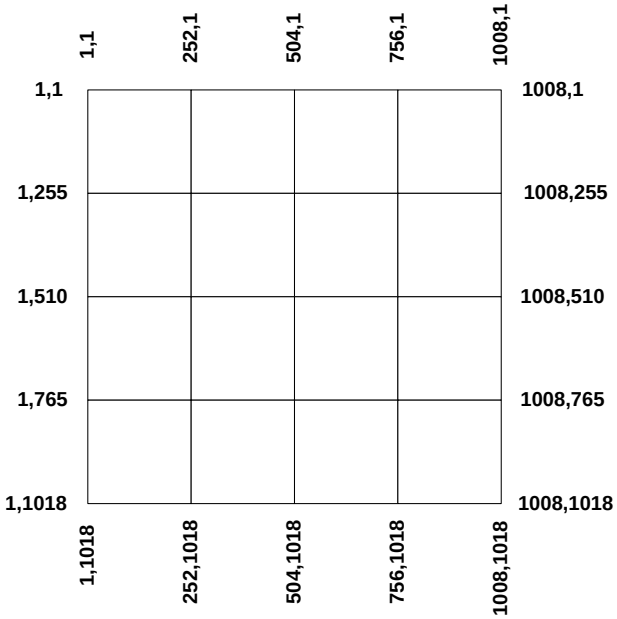
Defect Classification

All values derived under nominal operating conditions at 40 °C operating temperature.

Defect Type	Defect Definition	Number Allowed	Notes
Defective Pixel	Under uniform illumination with mean pixel output at 80% of Vsat, a defective pixel deviates by more than 15% from the mean value of all pixels in its section.	12	1
Bright Defect	Under dark field conditions, a bright defect deviates more than 15mV from the mean value of all pixels in its section.	5	1
Cluster Defect	Two or more vertically or horizontally adjacent defective pixels.	0	

Notes:

1. Sections are 252 (H) x 255 (V) pixel groups, which divide the imager into sixteen equal areas as shown below.



Test Conditions	
Junction Temperature	(T_j) = 40 °C
Integration Time	(t_{int}) = 70 msec
Readout Rate	($t_{readout}$) = 70 msec

Operation

Absolute Maximum Range

RATING	DESCRIPTION	MIN.	MAX.	UNITS	NOTES
Temperature (@ 10% ± 5%RH)	Operation Without Damage	-50	+70	°C	5, 6
Voltage (Between Pins)	SUB-WELL	0	+40	V	1, 7
	VRD,VDD,OG&VSS-WELL	0	+15	V	2
	IDHA,B & VOUTA,B - WELL	0	+15	V	2
	φV1 - φV2	-12	+20	V	2
	φH1A, φH1B - φH2	-12	+15	V	2
	φH1A, φH1B, φH2, FDG - φV2	-12	+15	V	2
	φH2 - OG & VSS	-12	+15	V	2
	φR – SUB	-20	0	V	1,2,4
	All Clocks - WELL	-12	+15	V	2
Current	Output Bias Current (I_{out})	----	10	mA	3

Table 5: Absolute Maximum Ranges

Notes:

1. Under normal operating conditions the substrate voltage should be above +7 V, but may be pulsed to 40 V for electronic shuttering.
2. Care must be taken in handling so as not to create static discharge which may permanently damage the device.
3. Per Output. I_{out} affects the band-width of the outputs.
4. φR should never be more positive than VSUB.
5. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
6. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
7. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

DC Operating Conditions

SYMBOL	DESCRIPTION	MIN.	NOM.	MAX.	UNITS	PIN IMPEDANCE6	NOTES
VRD	Reset Drain	8.5	9	9.5	V	5 pF, > 1.2 MΩ	
IRD	Reset Drain Current		0.2		mA		
VSS	Output Amplifier Return & OG		0		V	30 pF, >1.2 MΩ	
ISS	Output Amplifier Return Current		5		mA		
VDD	Output Amplifier Supply	12	15.0	15.0	V	30 pF, >1.2 MΩ	
Iout	Output Bias Current		5	10	mA		5
WELL	P-well	----	0.0	----	V	Common	1
GND	Ground	-----	0.0	----	V		1
FDG	Fast Dump Gate	-7.0	-6.0	-5.5	V	20 pF, >1.2 MΩ	2
SUB	Substrate	7	Vsub	15	V	1 nF, >1.2 MΩ	3, 8
IDHA, IDHB	Input Diode A, B Horizontal CCD	12.0	15.0	15.0	V	5 pF, > 1.2 MΩ	4

Table 6: DC Operating Conditions

Notes:

1. The WELL and GND pins should be connected to P-well ground.
2. The voltage level specified will disable the fast dump feature.
3. This pin may be pulsed to Ves=40 V for electronic shuttering
4. Electrical injection test pins. Connect to VDD power supply.
5. Per output. Note also that I_{out} affects the bandwidth of the outputs.
6. Pins shown with impedances greater than 1.2 Mohm are expected resistances. These pins are only verified to 1.2 Mohm.
7. The operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

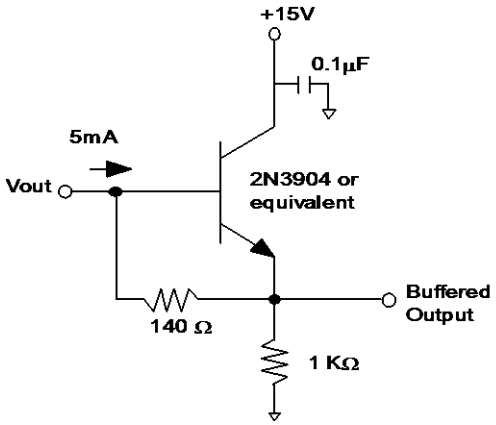


Figure 10: Recommended Output Structure Load Diagram

AC Clock Level Conditions

SYMBOL	DESCRIPTION	Level	Min.	NOM.	MAX.	UNITS	PIN IMPEDANCE[2]
φV1	Vertical CCD Clock	Low	-10.0	-9.5	-9.0	V	25 nF, >1.2 MΩ
		Mid	0.0	0.2	0.4	V	
		High	8.5	9.0	9.5	V	
φV2	Vertical CCD Clock	Low	-10.0	-9.5	-9.0	V	25 nF, >1.2 MΩ
		High	0.0	0.2	0.4	V	
φH1A	φ1 Horizontal CCD A Clock	Low	-7.5	-7.0	-6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
φH1B[4]	φ1 Horizontal CCD B Clock (single register mode)	Low	-7.5	-7.0	-6.5	V	100 pF, > 1.2 MΩ
φH1B[4]	φ1 Horizontal CCD B Clock (dual register mode)	Low	-7.5	-7.0	-6.5	V	100 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
φH2	φ2 Horizontal CCD Clock	Low	-7.5	-7.0	-6.5	V	125 pF, > 1.2 MΩ
		High	2.5	3.0	3.5	V	
φR	Reset Clock	Low	-6.5	-6.0	-5.5	V	5 pF, > 1.2 MΩ
		High	-0.5	0.0	0.5	V	
φFDG[3]	Fast Dump Gate Clock	Low	-7.0	-6.0	-5.5	V	20 pF, > 1.2 MΩ
		High	4.5	5.0	5.5	V	

Table 7: AC Clock Level Conditions

Notes:

1. The AC and DC operating levels are for room temperature operation. Operation at other temperatures may or may not require adjustments of these voltages.
2. Pins shown with impedances greater than 1.2 Mohm are expected resistances. These pins are only verified to 1.2 Mohm.
3. When not used, refer to DC operating condition.
4. For single register mode, set φH1B to -7.0 volts at all times rather than clocking it.
5. This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Truesense Imaging in those situations in which operating conditions meet or exceed minimum or maximum levels.

AC Timing Requirements for 20 MHz Operation

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNITS	NOTES	FIGURE
tφR	Reset Pulse Width		10		nsec		Figure 10
t es	Electronic Shutter Pulse Width	10	25		µsec		Figure 11
t int	Integration Time	0.1			msec	1	Figure 11
t φVh	Photodiode to VCCD Transfer Pulse Width	4	5		µsec	2	Figure 8
t cd	Clamp Delay		15		nsec		Figure 10
t cp	Clamp Pulse Width		15		nsec		Figure 10
t sd	Sample Delay		35		nsec		Figure 10
t sp	Sample Pulse Width		15		nsec		Figure 10
t rd	Vertical Readout Delay	10	----	----	µsec		Figure 8
t φV	φV1, φV2 Pulse Width	3	----		µsec		Figure 9
t φH	Clock Frequency φH1A, φH1B , φH2	----	20		MHz		Figure 10
t φAB	Line A to Line B Transfer Pulse Width		3		µsec		Figure 13
t φHd	Horizontal Delay	3			µsec		Figure 9
t φVd	Vertical Delay	25			nsec		Figure 9
t φHVES	Horizontal Delay with Electronic Shutter	1			µsec		Figure 11

Table 8: AC Timing Requirements for 20 MHz Operation

Notes:

1. Integration time varies with shutter speed. It is to be noted that smear increases when integration time decreases below readout time (frame time). Photodiode dark current increases when integration time increases, while CCD dark current increases with readout time (frame time).
2. Antiblooming function is off during photodiode to VCCD transfer.

Frame Timing - Single Register Readout

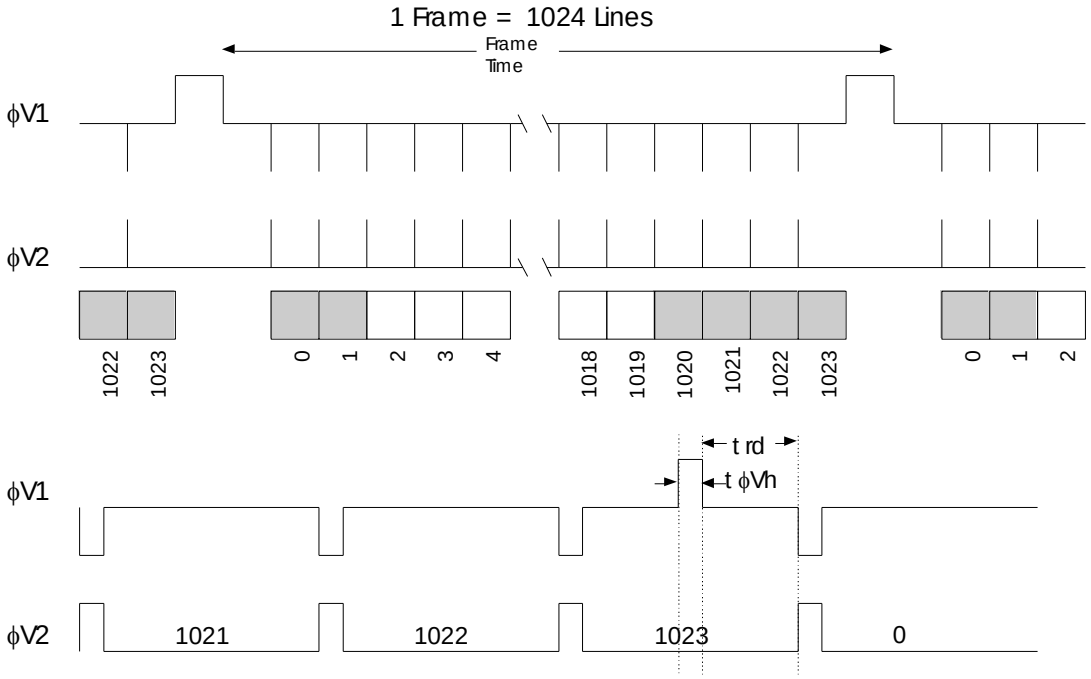
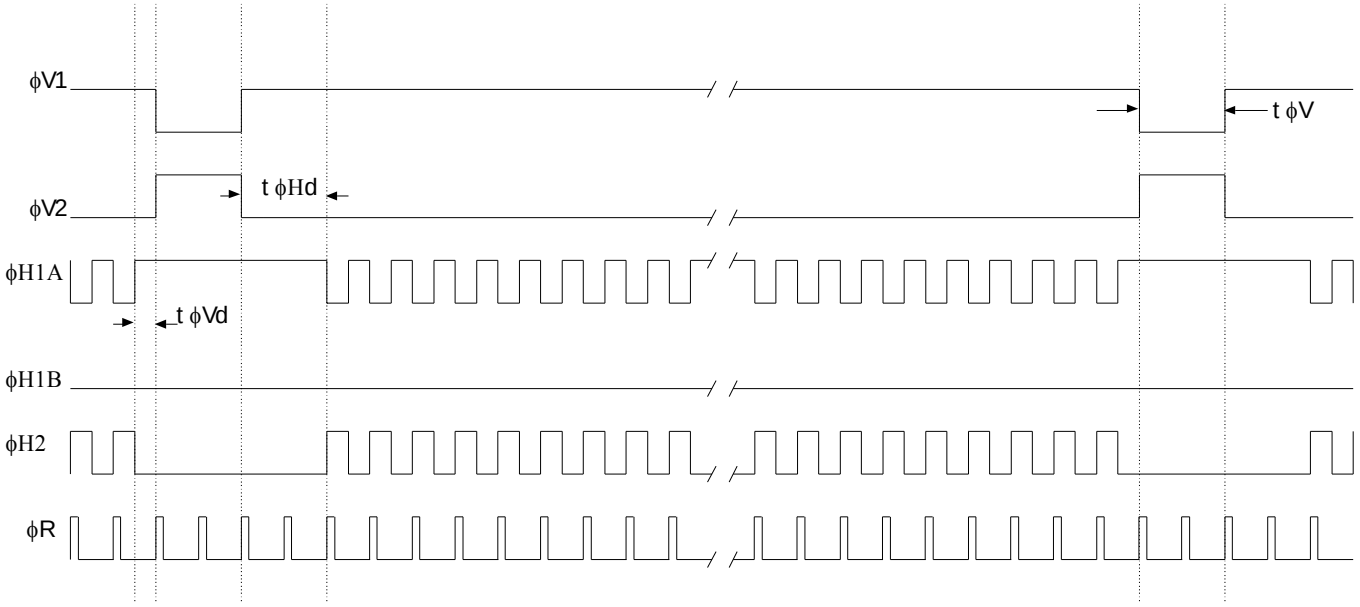


Figure 11: Frame Timing - Single Register Readout

Note:

1. When no electronic shutter is used, the integration time is equal to the frame time.

Line Timing - Single Register Readout



H1B held low for single register operation

Line Content

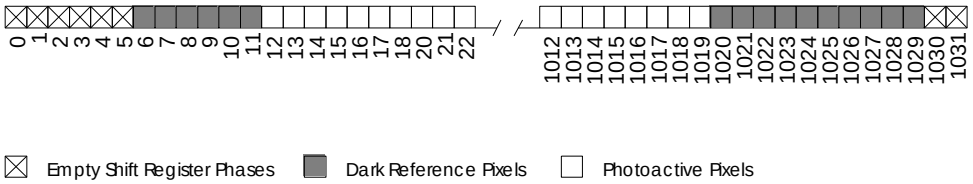


Figure 12: Line Timing - Single Register Output

Pixel Timing - Single Register Readout

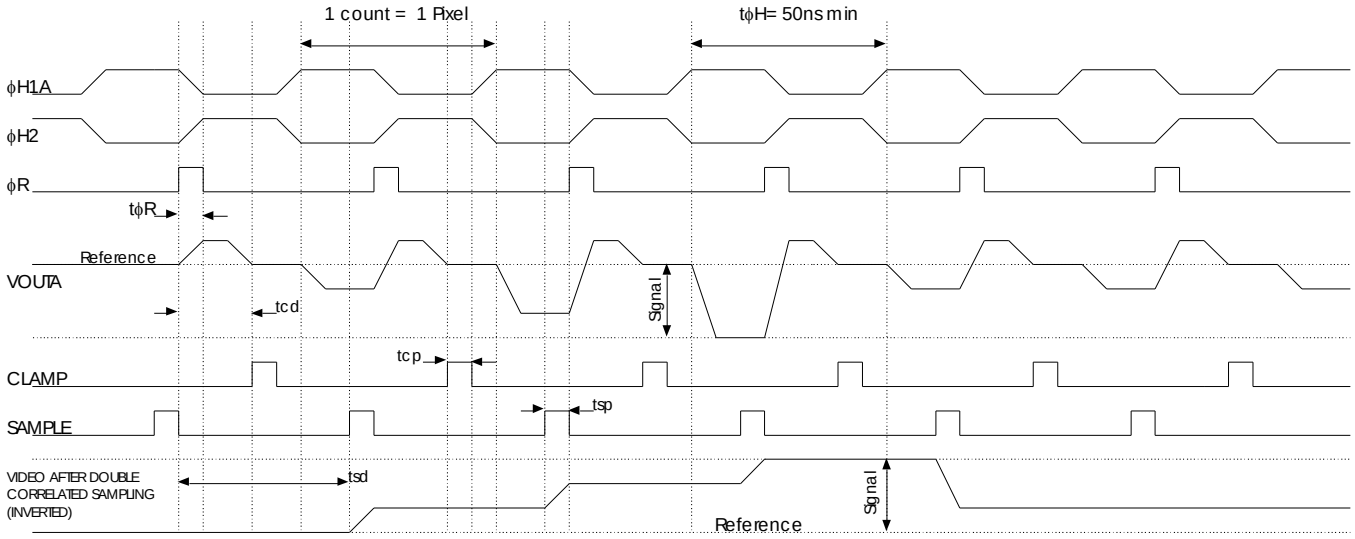
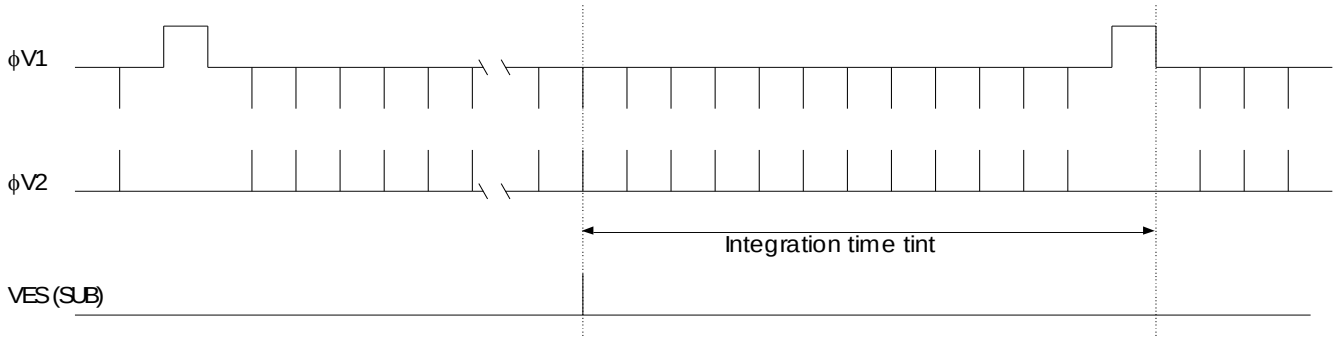


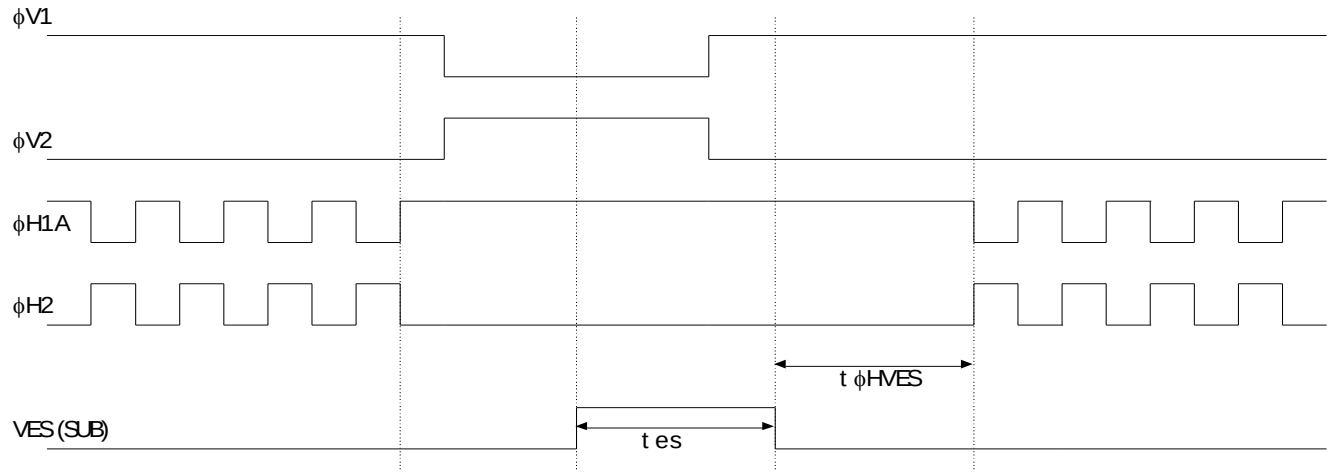
Figure 13: Pixel Timing Diagram - Single Register Readout

Electronic Shutter Timing - Single Register Readout

Electronic Shutter - Frame Timing



Electronic Shutter - Placement



Electronic Shutter - Operating Voltages

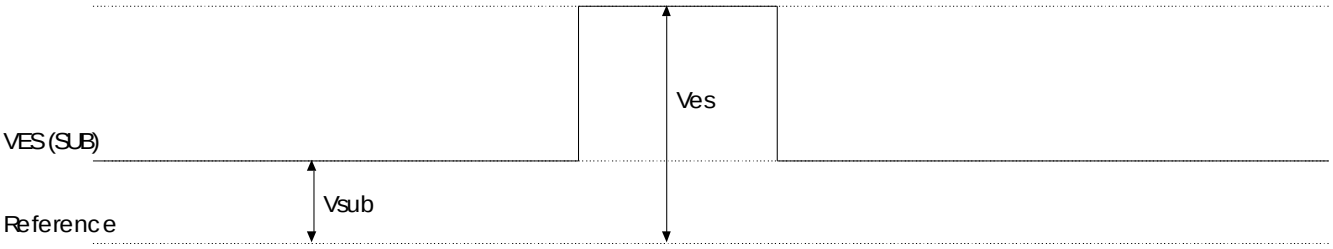


Figure 14: Electronic Shutter Timing Diagram - Single Register Readout

Frame Timing - Dual Register Readout

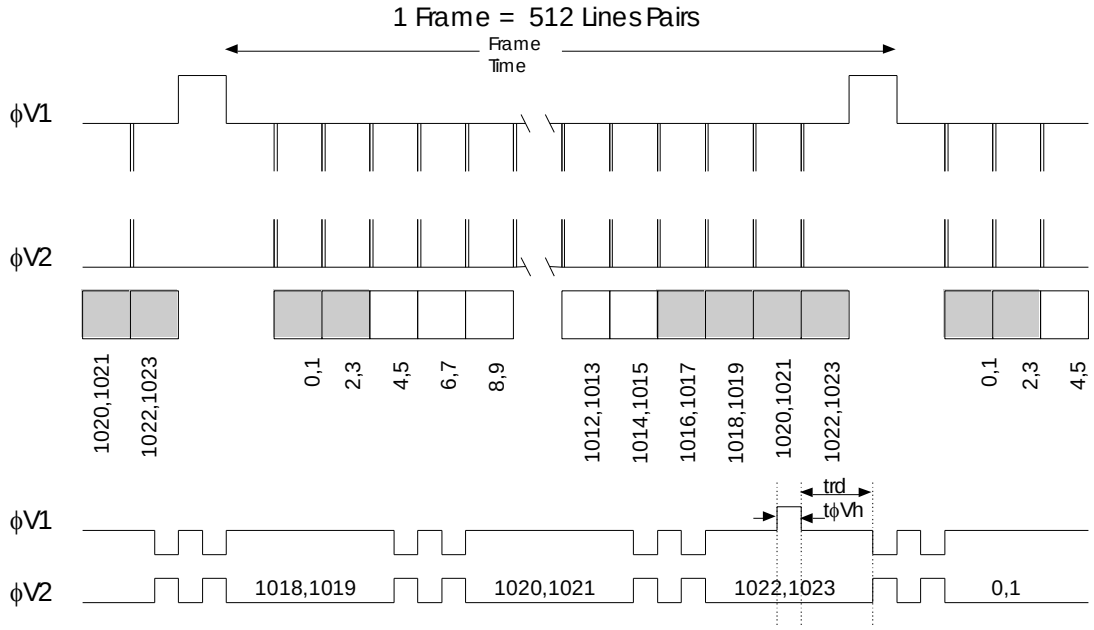
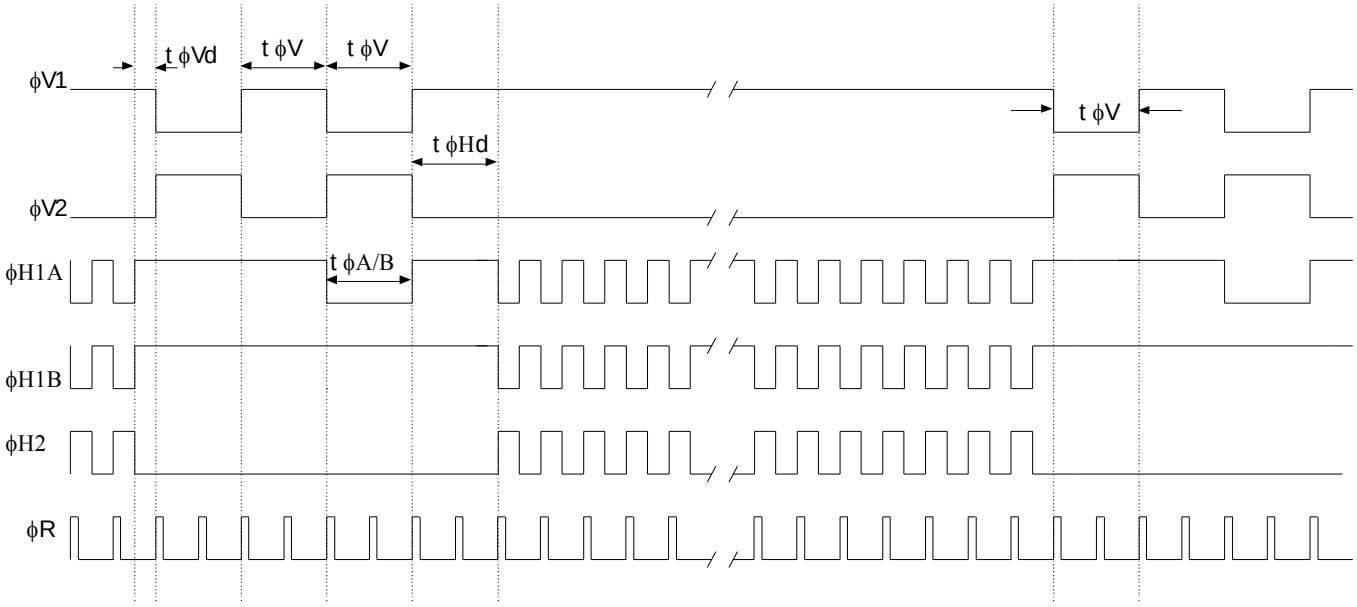


Figure 15: Frame Timing - Dual Register Readout

Note:

1. When no electronic shutter is used, the integration time is equal to the frame time.

Line Timing - Dual Register Readout



Line Content

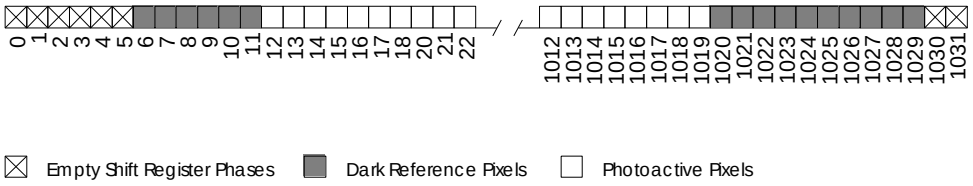


Figure 16: Line Timing - Dual Register Output

Pixel Timing - Dual Register Readout

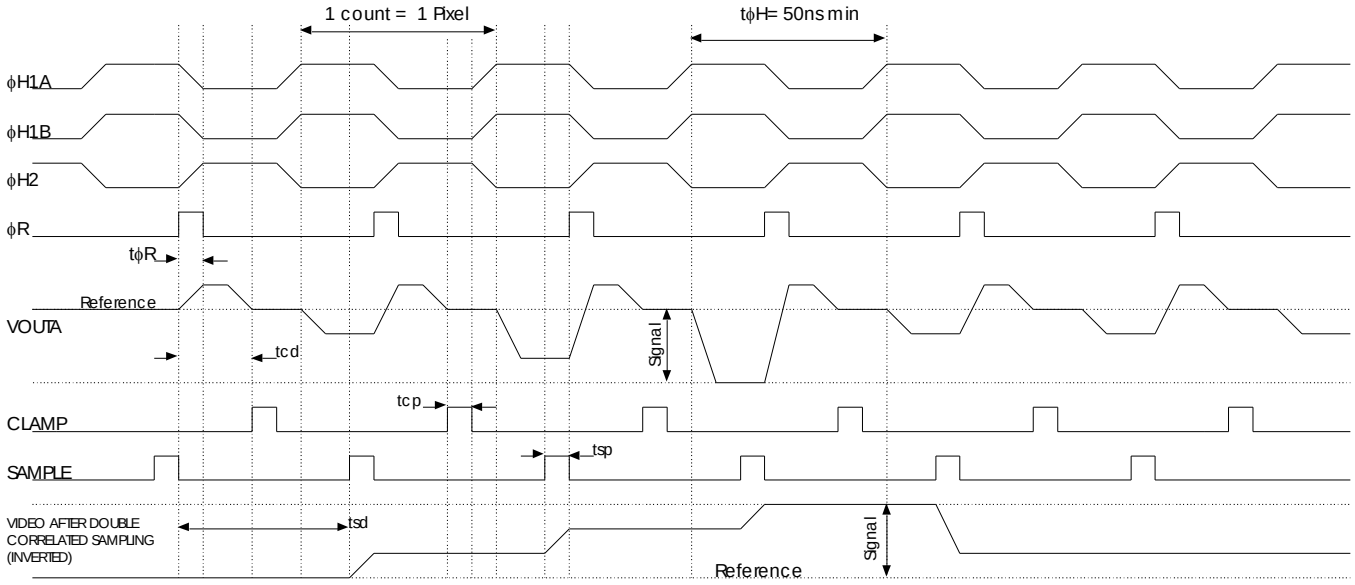


Figure 17: Pixel Timing Diagram - Dual Register Readout

Fast Dump Timing – Removing Four Lines

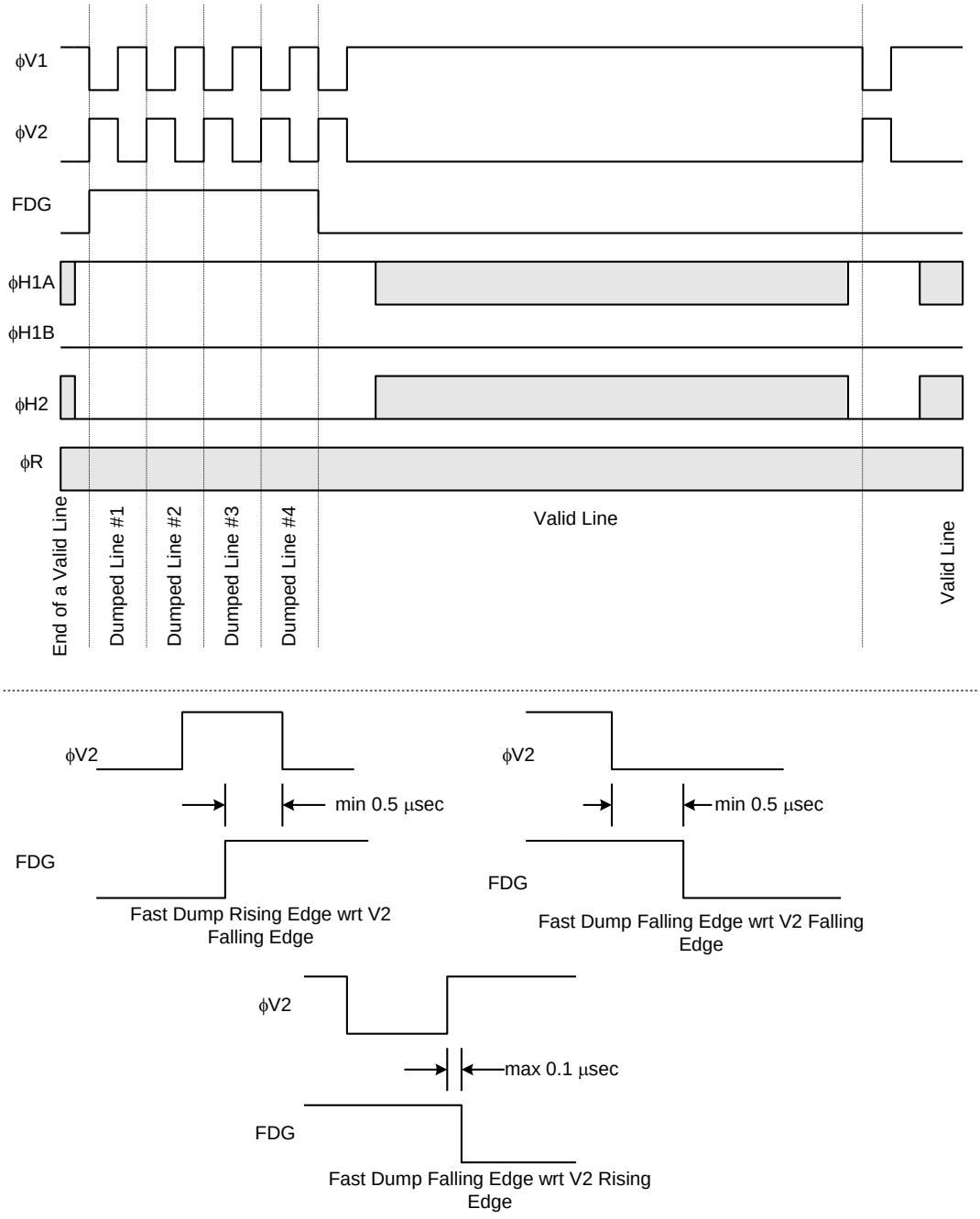


Figure 18: Fast Dump Timing - Removing Four Lines

Binning – Two to One Line Binning

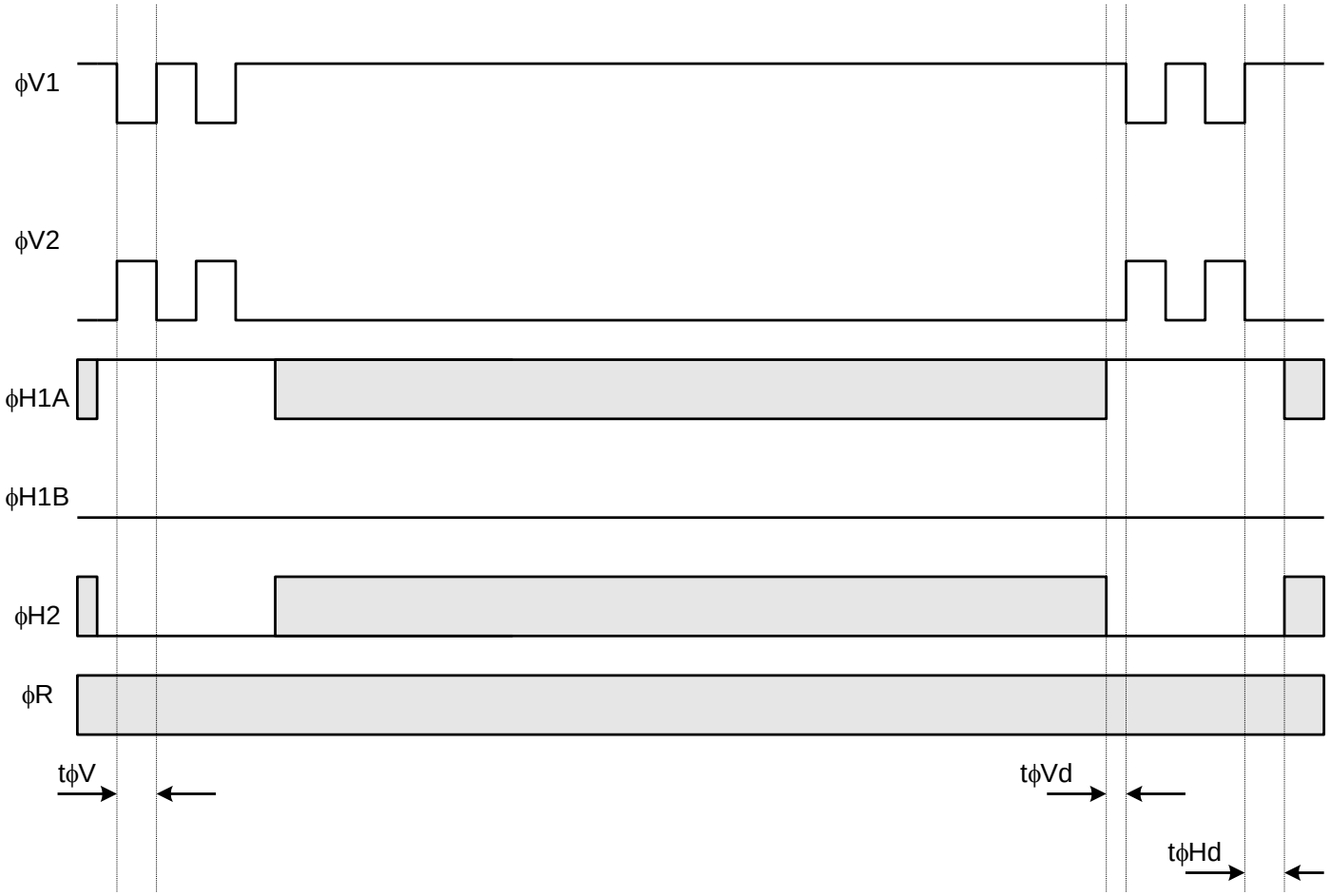


Figure 19: Binning - 2 to 1 Line Binning

Timing – Sample Video Waveform

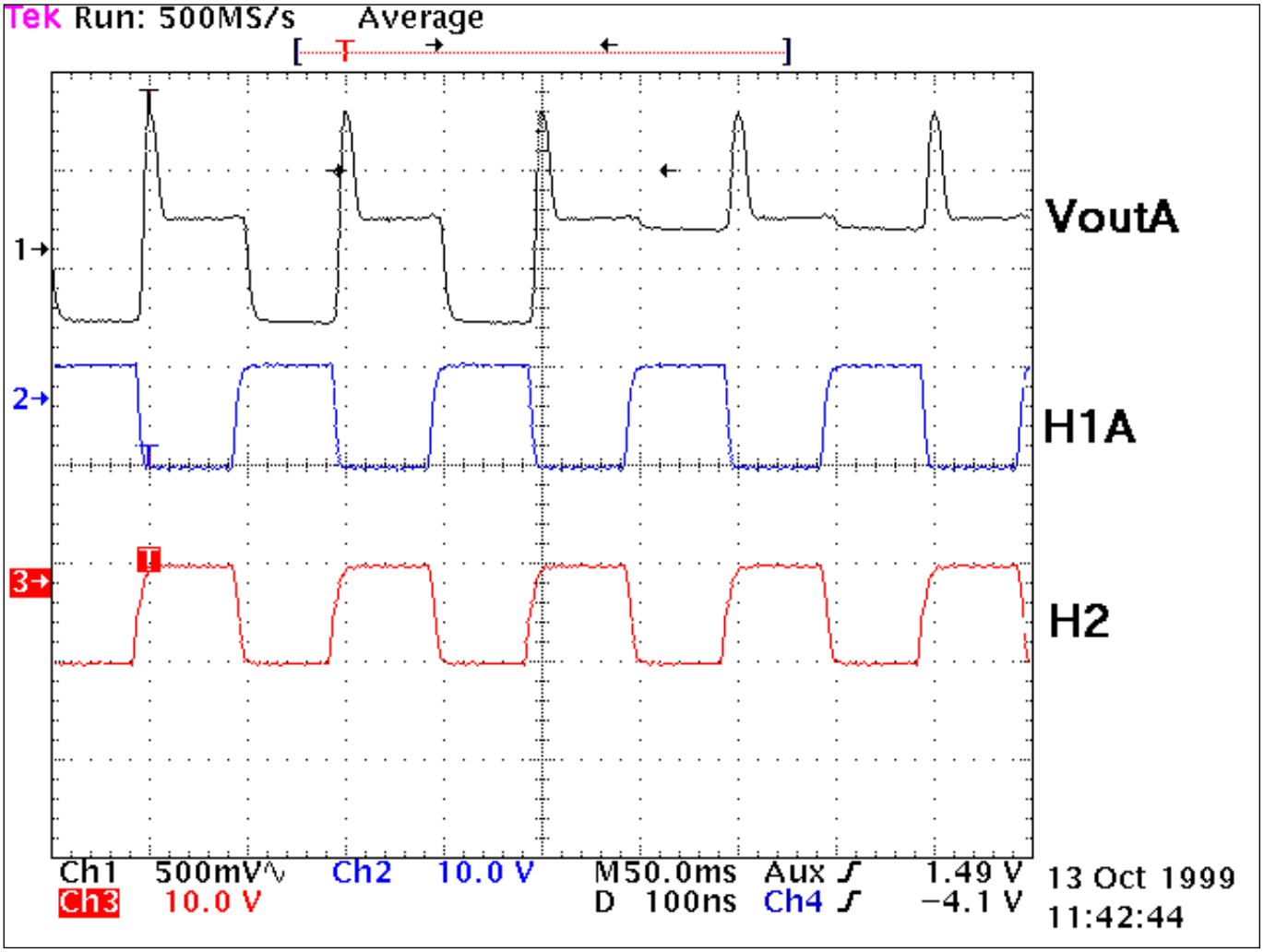


Figure 20: Sample Video Waveform at 5MHz

Storage and Handling

Climatic Requirements

ITEM	DESCRIPTION	MIN.	MAX.	UNITS	CONDITIONS	NOTES
Operation to Specification	Temperature	-25	+40	°C	@ 10% ± 5% RH	1, 2
	Humidity	10	86	%RH	@ 36 ± 2 °C Temp.	1, 2
Storage	Temperature	-55	+70	°C	@ 10% ± 5%RH	2, 3
	Humidity	-----	95	%RH	@ 49 ± 2 °C Temp.	2, 3

Table 9: Climatic Requirements

Notes:
1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
3. The image sensor shall meet the specifications of this document after storage for 15 days at the specified condition

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.

4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

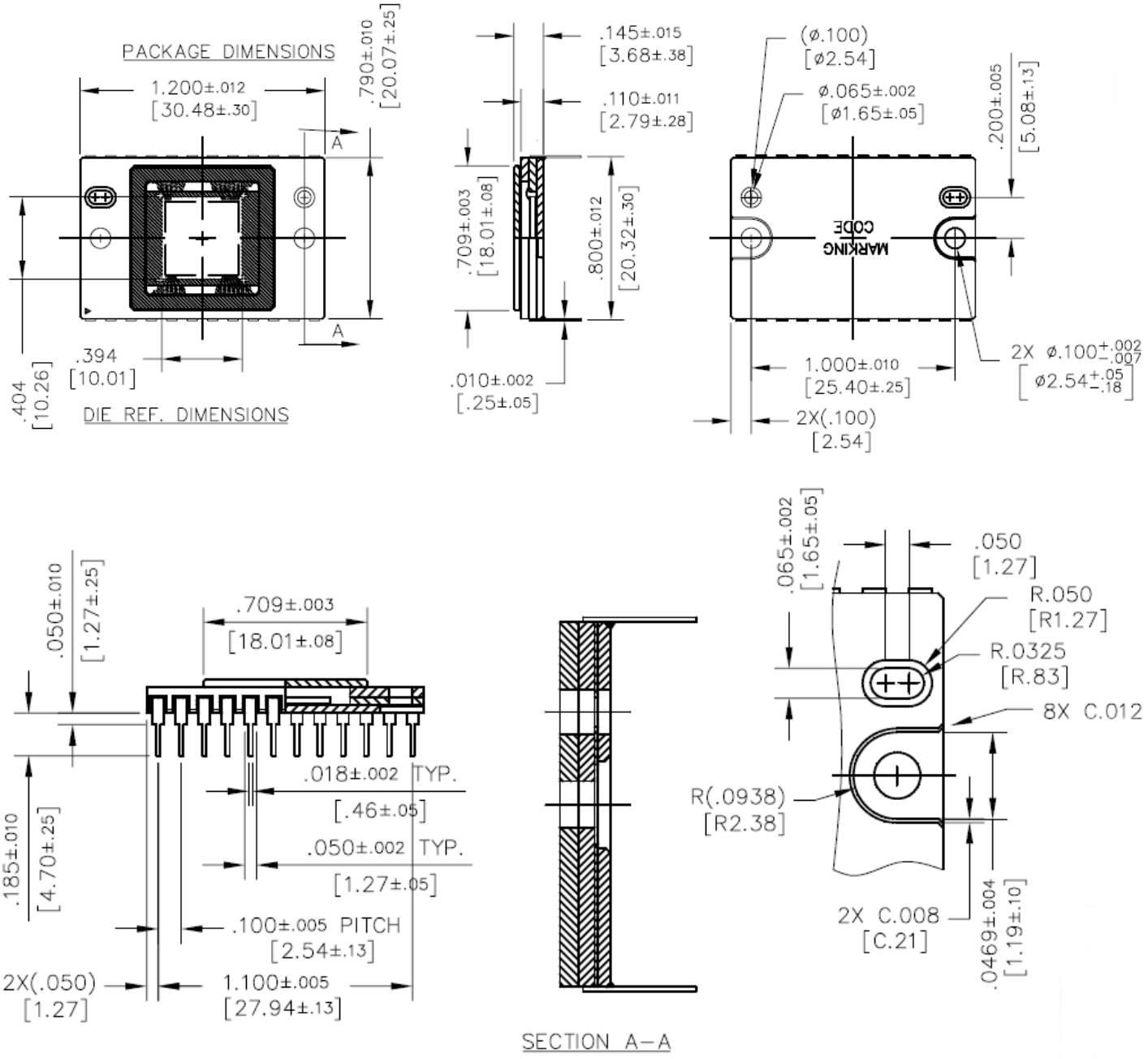


Figure 21: Completed Assembly (1 of 2)

Notes:

1. Cover glass is manually placed and visually aligned over die – location accuracy is not guaranteed.

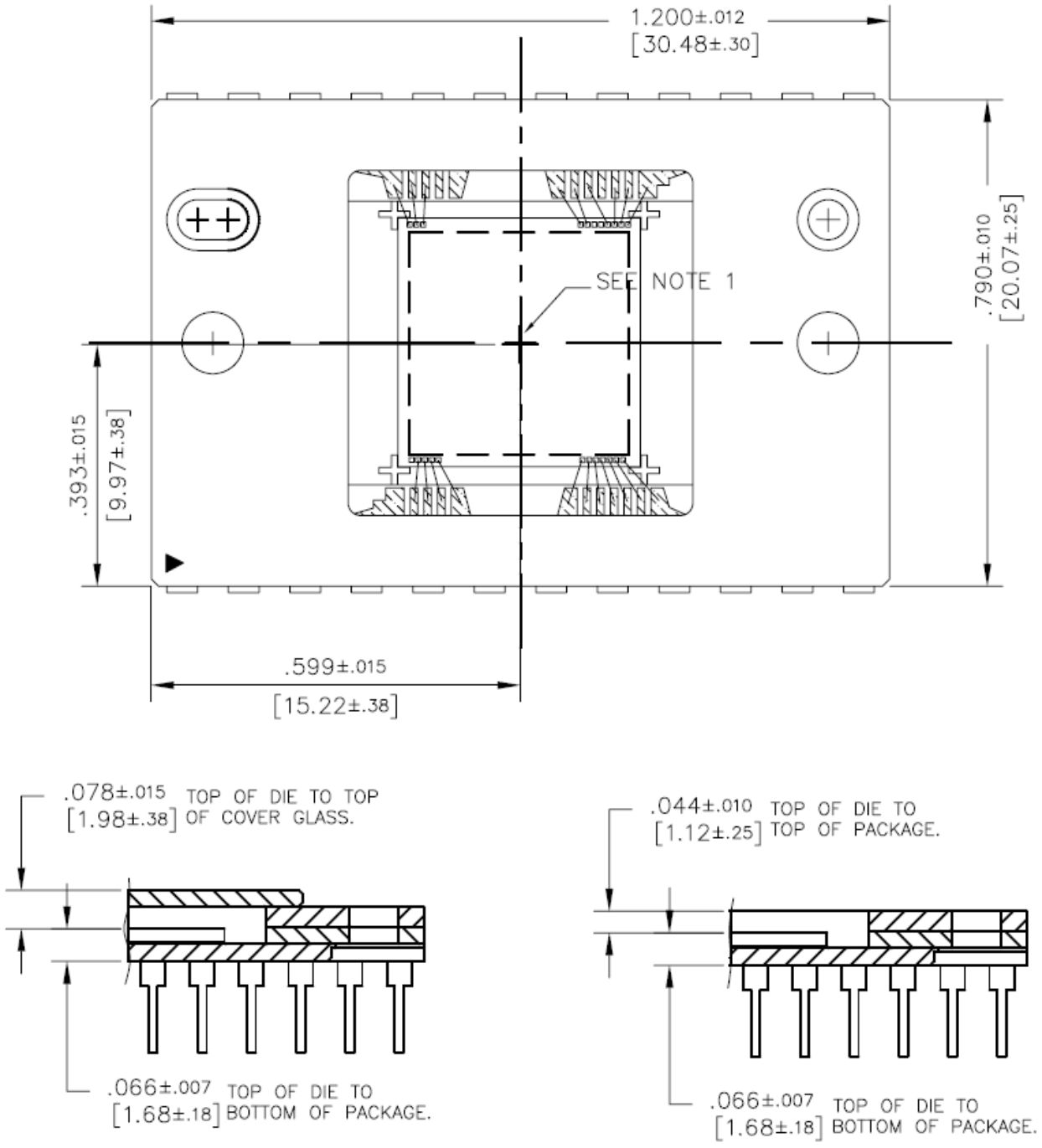


Figure 22: Completed Assembly (2 of 2)

Notes:

1. Center of image area is offset from center of package by (-0.02, -0.06) mm nominal.
2. Die is aligned within +/- 2 degree of any package cavity edge.

COVER GLASS

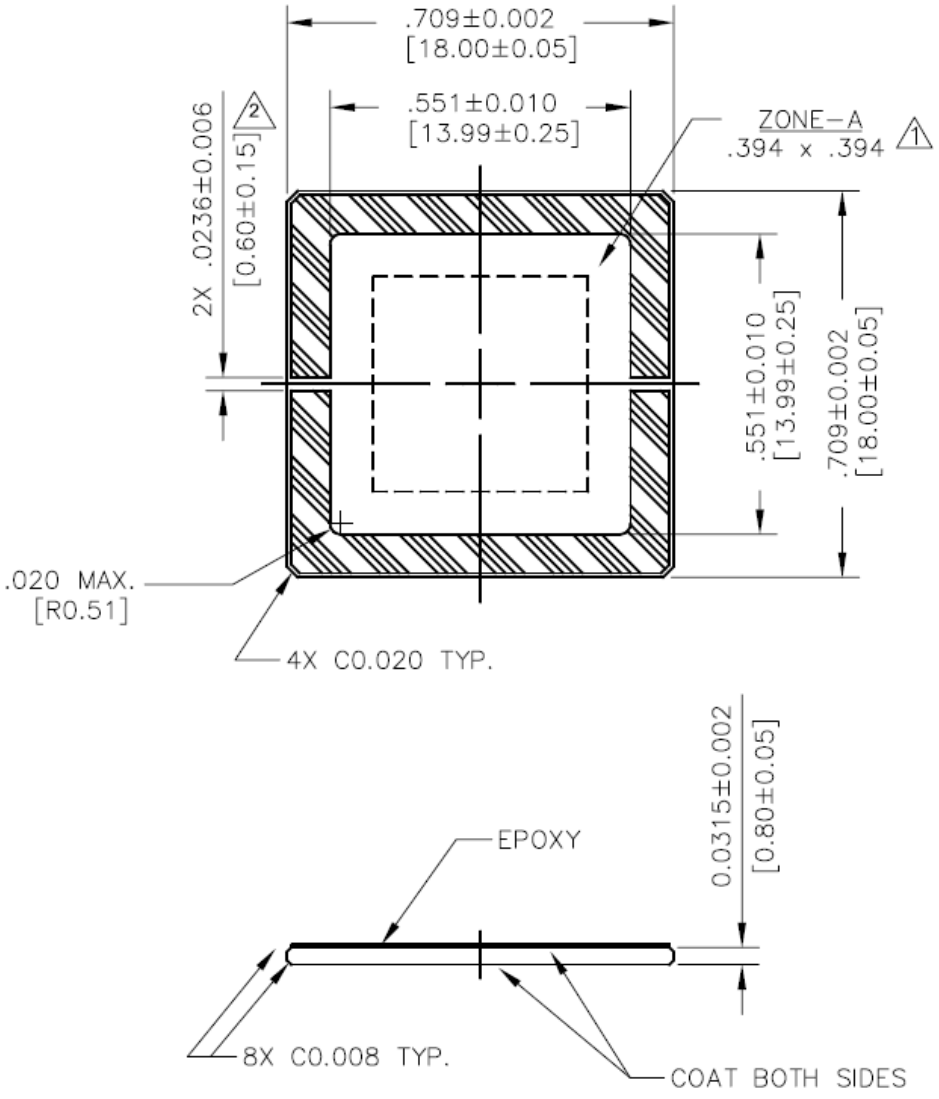


Figure 23: Glass Drawing

Notes:

1. DUST/SCRATCH COUNT – 20 MICRON MAX. (ZONE-A)
2. EPOXY: NCO-110SZ
   THICKNESS: 0.002" – 0.007"
3. GLASS: SCHOTT D263 eco or equivalent
4. DOUBLE-SIDED AR COATING REFLECTANCE
   a. 420nm – 435nm < 2.0%
   b. 435nm – 630nm < 0.8%
   c. 630nm – 680nm < 2.0%

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0502

Revision Number	Description of Revision
0.0	• Revision 0 is the original version of the document
1.0	• Revision 1.0 changes name from KAI-1001C to KAI-1001 series and includes data on all series imagers
2.0	• Entire spec revised
3.0	• Entire spec revised
4.0	• Changed from KAI-1001 series to KAI-1010. Added cluster closeness specification, 4 good pixels between cluster defects.
5.0	• Changed defect and grades. • Added frame rate table and angle QE.
6.0	• Added Web and e-mail references to footers. • Added pixel 1,1 locator to figure 7, Pinout diagram. • Corrected missing reference to figure 16 in Electro-Optical for KAI-1010CM note 2. • Removed reference to KAI-1001 from both color and mono QE curves. • Removed boxes around vertical and horizontal labels on angle QE figure. • Removed boxes around labels on frame rate figure, added arrows from labels to curves. • Corrected figure 21 Vsat versus Vsub plot to properly position labels. • Added Web and e-mail references in section 4.3 ordering information. • Corrected repeat table 4 entry. • Corrected frame rate versus horizontal clock frequency figure. Data for dual mode was incorrect.
7.0	• Changed figure 6 label from Device Drawing #6 Die Placement to Device Drawing – Die Placement. • Added figure 16, Fast Dump Timing. • Added figure 17, Binning – 2 to 1 line binning. • Added figure 18, Sample Video Waveform at 5MHz. • In Appendix 1, Part Numbers, changed references from taped on glass to snap-on lid.
8.0	• Updated page layout. • Color version of part updated to use improved material. Naming of color part changed from KAI-1010CM to KAI-1011CM. • Page 13 – Added cautions pertaining to ESD and glass cleaning. • Page 26 – Color PRNU value changed from 5 to 15. Units clarified to % Peak to Peak. • Page 28 – Monochrome PRNU value changed from 5 to 10. Units clarified to % Peak to Peak. • Page 27 – Updated color quantum efficiency graph to new KAI-1011CM. • Page 35 – Updated quality Assurance and Reliability section. • Page 36 – Appendix 1 replaced with Available Part Configurations.
9.0	• Page 8 – Figure 5 – CFA Pattern – corrected pattern. First active line is blue/green. Previous versions on the specification incorrectly had the first active line as green/red. • Note: the color filter pattern has not been physically changed on the device. • Page 35 – Update Storage and Handling Section. • Page 36 – Updated Quality Assurance and Reliability section.
10.0	• Page 37 – removed KAI-1010 monochrome sealed quartz glass configuration. This configuration has been obsoleted.
11.0	• Updated format • Updated Summary Specification • Updated completed assembly drawing • Added cover glass drawing • Updated ordering information
12.0	• Obsoleted KAI-1011-CBA and KAI-1010-AAA products

13.0	• Added the note "Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*" to the following sections
	  ○ Electronic Shutter
	  ○ Absolute Maximum Ratings
	  ○ DC Operating Conditions
	  ○ Storage and Handling
	• Changed cover glass material to D263T eco or equivalent

PS-0021

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections
1.1	• Updated branding

PUBLICATION ORDERING INFORMATION

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